

# SYSTEM AND METHOD FOR IMPROVED SYNCHRONOUS DATA ACCESS

## Abstract of the Disclosure

A system and method for improved synchronous access of stored data are provided herein. A data requestor transmits a clock signal and a read request signal for reception by a data source, whereupon skewed versions of the clock signal and the read request signal are received due to the delays in the signal paths between the data requestor and the data source. Accordingly, the data requestor provides skewed clock and read request signals to its input sampling module to simulate the delays of the signal paths. Additionally, the data requestor provides process information associated with the requested data to a dual clock first in–first out (FIFO) buffer. When the input sampling module detects a read request using the skewed read request signal, the input sampling module can use this signal and the skewed clock signal to sample a data signal from the data source to obtain the requested data. Concurrently, the input sampling module can access the process information from the dual clock FIFO buffer using the skewed clock signal. Based at least in part on this process information, one or more process operations can be performed on the requested data. In other implementations, the storage and subsequent access of process information from a dual–clock FIFO is omitted. The present invention finds particular benefit in accessing data stored in synchronous memory, such as synchronous dynamic random access memory (SDRAM) and synchronous static random access memory (SSRAM).

